library of groups, each group having a predefined logical and physical layout, and having a plurality of layers within which intra-group interconnections are provided among various elements within the group, the physical layout having predefined boundaries with predefined interconnection points, and at least some of the groups being amalgamated into functions, the functions being present in a library of functions, the method comprising:

when the intra-group interconnections are defined, providing all such interconnections on fewer than all of the plurality of layers;

selecting an item, the item being a group or a function, for placement on a layout;

placing the item on the layout;

selecting a further item for placement on the layout;

placing the further item on the layout; and

defining inter-group interconnections between the item and the further item, the inter-group interconnections being provided entirely on layers that are not used for the intra-group interconnections.

Please cancel claim 12 without prejudice.

Please amend claims 13, 14 and 19-21 as follows:

13. (Amended) The method of claim 11 wherein the plurality of layers are each layers having electrically conductive material thereon, with vias from at least one adjoining layer connected thereto.

14. (Amended) An integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points, each group having interconnections within that group on a plurality of layers of the integrated circuit, the

A2 cont'd

plurality of layers being less than all of the layers, at least some of the circuit groups being amalgamated into sets of groups.

19. (Amended) The integrated circuit of claim 14 wherein the plurality of circuit groups are provided to have electrical connections within them solely on a first plurality of electrically conductive layers, and wherein clock and power signals are provided on electrically conductive layers other than the first plurality of electrically conductive layers.

A3

20. (Amended) The integrated circuit of claim 19 wherein the clock and power signals are on the same layer.

21. (Amended) The integrated circuit of claim 20 wherein global routing signals among the plurality of groups are transferred among the groups on at least one electrically conductive layer other than the first plurality of electrically conductive layers or the layer used for the clock and power signals.